CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for detecting a mismatch in a content addressable memory (CAM), the method comprising:

charging a matchline of a match detection circuit of said CAM to a first voltage level;

comparing a logic state of a first bit stored in said CAM with a logic state of a second bit received at said CAM; and

changing the voltage level of said matchline to a second voltage level if the logic state of the first bit does not match the logic state of the second bit, said second voltage level being different than said first voltage level and different than a ground potential.

2. The method of claim 1, wherein said act of charging comprises:

precharging said matchline to said first voltage level before said second bit is received at said CAM.

3. The method of claim 2, wherein said act of precharging comprises precharging said matchline to VDD.

4. The method of claim 2, wherein said act of precharging comprises precharging said matchline to a negative reference voltage level lower than VDD.

5. The method of claim 1, wherein said act of comparing comprises:

comparing said logic state of said first bit with a logic state of a complement of said second bit; and

comparing a logic state of a complement of said first bit with said logic state of said second bit.

6. The method of claim 5, wherein said first act of comparing comprises:

receiving said logic state of said first bit at a gate of a first transistor; and

receiving said logic state of said complement of said second bit at a gate of a second transistor in series with said first transistor, wherein if said logic state of said first bit matches said complement of said logic state of said second bit, said first and second transistors are activated and conducting.

7. The method of claim 5, wherein said second act of comparing comprises:

receiving said logic state of said complement of said first bit at a gate of a third transistor; and

receiving said logic state of said second bit at a gate of a fourth transistor in series with said third transistor, wherein if said logic state of said complement of said first bit matches said logic state of said second bit, said third and fourth transistors are activated and conducting.

8. The method of claim 6, wherein said act of changing comprises coupling said matchline, via said first and second transistors, to a terminal having a voltage level lower than said first voltage level and a voltage level higher than a ground potential.

9. The method of claim 7, wherein said act of changing comprises coupling said matchline, via said third and fourth transistors, to a terminal having a voltage level lower than said first voltage level and a voltage level higher than a ground potential.

10. A method for detecting a mismatch in a content addressable memory (CAM), the method comprising:

charging a matchline of a match detection circuit of said CAM to a first voltage level;

respectively comparing logic states of a first plurality of bits stored in said CAM with respective logic states of a second plurality of bits received at said CAM, each of said second plurality of bits having a corresponding bit in said first plurality of bits; and

changing the voltage level of said matchline to a second voltage level if the logic state of at least one of said second plurality of bits does not match the logic state of its corresponding bit in said first plurality of bits, said second voltage level being different than said first voltage level and higher than a ground potential.

11. The method of claim 10, wherein said act of charging comprises:

precharging said matchline to said first voltage level before said second plurality if bits is received at said CAM.

12. The method of claim 11, wherein said act of precharging comprises precharging said matchline to VDD.

13. A match detection circuit for a content addressable memory (CAM), comprising:

a matchline configured to have a first logic state when a match is detected between a logic state of a bit stored in said CAM and a logic state of a bit received by said CAM, and configured to have a second logic state when a mismatch is detected between the logic states of said stored and received bits;

a first voltage terminal switchably coupled to said matchline for precharging said matchline to a first voltage level representing said first logic state; and

a second voltage terminal switchably coupled to said matchline for changing the logic state of said matchline from said first logic state to said second logic state, said second

voltage terminal having a voltage level different than said first voltage level and different than a ground voltage level.

14. The circuit of claim 13 further comprising a transistor coupled between said first voltage terminal and said matchline, said transistor being activated upon receipt of a precharge signal, thereby coupling said first voltage terminal with said matchline.

15. The circuit of claim 14, wherein said first voltage terminal comprises a VDD terminal.

16. The circuit of claim 13, wherein said second voltage terminal is connected to a regulated voltage source.

17. The circuit of claim 13, wherein said CAM comprises a storage element for storing said stored bit.

18. The circuit of claim 17, wherein said storage element comprises a flip-flop for storing a true logic state of said stored bit and a complementary logic state of said stored bit.

19. The circuit of claim 17 further comprising:

a first transistor, a gate of said first transistor coupled to said storage element for receiving said logic state of said stored bit, a first source/drain terminal of said first transistor being coupled to said matchline;

a second transistor, a gate of said second transistor configured to receive a complement of said bit received by said CAM, a first source/drain terminal of said second transistor being coupled to a second source/drain terminal of said first transistor, and a second source/drain terminal of said second transistor being coupled to said second voltage terminal;

a third transistor, a gate of said third transistor coupled to said storage element for receiving a complement of said logic state of said stored bit, a first source/drain terminal of said third transistor being coupled to said matchline;

a fourth transistor, a gate of said fourth transistor being configured to receive said logic state of said bit received by said CAM, a first source/drain terminal of said fourth terminal being coupled to a second source/drain terminal of said third transistor, a second source/drain terminal of said fourth transistor being coupled to said second voltage terminal.

20. The circuit of claim 19, wherein said first through fourth transistors comprise metal oxide semiconductor (MOS) transistors.

21. The circuit of claim 20, wherein said MOS transistors comprise p-type MOS transistors.

22. The circuit of claim 20, wherein said MOS transistors comprise n-type MOS transistors.

23. A match detection circuit for a content addressable memory (CAM), comprising:

a matchline switchably coupled between a first voltage terminal and a second voltage terminal, said first voltage terminal serving to precharge said matchline to a first voltage;

said matchline being configured to be connected to a second voltage level of said second terminal when a logic state of a bit stored by said CAM does not match a logic state of a bit received by said CAM for comparison with said stored bit, wherein said second voltage is greater than a ground potential and wherein said second voltage is lower than said first voltage.

24. A match detection circuit for a content addressable memory (CAM), comprising:

a plurality of stored bits to be compared with a corresponding plurality of input bits received by said CAM;

a matchline switchably coupled between a first voltage terminal and a second voltage terminal, said first voltage terminal serving to precharge said matchline to a first voltage level prior to said stored bits and said input bits being compared;

said matchline being coupled to said second voltage terminal when a logic state of at least one of said plurality of input bits does not match a logic state of a stored bit corresponding to said at least one input bit, said second voltage level being lower than said first voltage level and higher than a ground potential.

25. The circuit of claim 24 further comprising:

an output for outputting a first logic state when said plurality of stored bits matches said corresponding plurality of input bits received by said CAM, and for outputting a second logic state when said plurality of stored bits does not match said corresponding plurality of input bits received by said CAM.

26. The circuit of claim 25, wherein said first logic state is logic HIGH and wherein said second logic state is logic LOW.

27. The circuit of claim 24, wherein said first voltage level is VDD.

28. The circuit of claim 25, wherein said output comprises a buffer coupled to said matchline.

29. A semiconductor memory chip, comprising:

a plurality of match detection circuits for a content addressable memory (CAM), each of said match detection circuits comprising:

a matchline configured to have a first logic state when a match is detected between a logic state of a bit stored in said CAM and a logic state of a bit received by said CAM, and configured to have a second logic state when a mismatch is detected between the logic states of said stored and received bits;

a first voltage terminal switchably coupled to said matchline for precharging said matchline to a first voltage level representing said first logic state; and

a second voltage terminal switchably coupled to said matchline for changing the logic state of said matchline from said first logic state to said second logic state, said second voltage terminal having a voltage level different than said first voltage level and different than a ground voltage level.

30. The memory chip of claim 29, each of said match detection circuits further comprising a transistor coupled between said first voltage terminal and said matchline, said transistor being activated upon receipt of a precharge signal, thereby coupling said first voltage terminal with said matchline.

31. The memory chip of claim 30, wherein said first voltage terminal comprises a VDD terminal.

32. The memory chip of claim 29, wherein said second voltage terminal is connected to a regulated voltage source.

33. The memory chip of claim 29, wherein said CAM comprises a storage element for storing said stored bit.

34. The memory chip of claim 33, wherein said storage element comprises a flip-flop for storing a true logic state of said stored bit and a complementary logic state of said stored bit.

35. The circuit of claim 33, wherein each of said match detection circuits further comprise:

a first transistor, a gate of said first transistor coupled to said storage element for receiving said logic state of said stored bit, a first source/drain terminal of said first transistor being coupled to said matchline;

a second transistor, a gate of said second transistor configured to receive a complement of said bit received by said CAM, a first source/drain terminal of said second transistor being coupled to a second source/drain terminal of said first transistor, and a second source/drain terminal of said second transistor being coupled to said second voltage terminal;

a third transistor, a gate of said third transistor coupled to said storage element for receiving a complement of said logic state of said stored bit, a first source/drain terminal of said third transistor being coupled to said matchline;

a fourth transistor, a gate of said fourth transistor being configured to receive said logic state of said bit received by said CAM, a first source/drain terminal of said fourth terminal being coupled to a second source/drain terminal of said third transistor, a second source/drain terminal of said fourth transistor being coupled to said second voltage terminal.

36. The memory chip of claim 35, wherein said first through fourth transistors comprise metal oxide semiconductor (MOS) transistors.

37. The memory chip of claim 36, wherein said MOS transistors comprise p-type MOS transistors.

38. The memory chip of claim 36, wherein said MOS transistors comprise n-type transistors.

39. A semiconductor memory chip, comprising:

a plurality of match detection circuits for a content addressable memory (CAM), each of said match detection circuits comprising:

a matchline switchably coupled between a first voltage terminal and a second voltage terminal, said first voltage terminal serving to precharge said matchline to a first voltage;

said matchline being configured to be connected to a second voltage level of said second terminal when a logic state of a bit stored by said CAM does not match a logic state of a bit received by said CAM for comparison with said stored bit, wherein said second voltage is greater than a ground potential and wherein said second voltage is lower than said first voltage.

40. A semiconductor chip, comprising:

a plurality of match detection circuits for a content addressable memory (CAM), each of said match detection circuits comprising:

a plurality of stored bits to be compared with a corresponding plurality of input bits received by said CAM;

a matchline switchably coupled between a first voltage terminal and a second voltage terminal, said first voltage terminal serving to precharge said matchline to a first voltage level prior to said stored bits and said input bits being compared;

said matchline being coupled to said second voltage terminal when a logic state of at least one of said plurality of input bits does not match a logic state of a stored bit corresponding to said at least one input bit, said second voltage level being lower than said first voltage level and higher than a ground potential.

41. The memory chip of claim 40, wherein each match detection circuit further comprises:

an output for outputting a first logic state when said plurality of stored bits matches said corresponding plurality of input bits received by said CAM, and for outputting a second logic state when said plurality of stored bits does not match said corresponding plurality of input bits received by said CAM.

42. The memory chip of claim 41, wherein said first logic state is logic HIGH and wherein said second logic state is logic LOW.

43. The memory chip of claim 41, wherein said first logic state is logic LOW and wherein said second logic state is logic HIGH.

44. A processor system, comprising:

a central processing unit;

a memory component coupled to said processor, said memory component containing a match detection circuit for a content addressable memory (CAM), said match detection circuit comprising:

a matchline configured to have a first logic state when a match is detected between a logic state of a bit stored in said CAM and a logic state of a bit received by said CAM, and configured to have a second logic state when a mismatch is detected between the logic states of said stored and received bits;

a first voltage terminal switchably coupled to said matchline for precharging said matchline to a first voltage level representing said first logic state; and

a second voltage terminal switchably coupled to said matchline for changing the logic state of said matchline from said first logic state to said second logic state, said second voltage terminal having a voltage level different than said first voltage level and higher than a ground voltage level.

45. The processor system of claim 44, wherein said match detection circuit further comprises:

a transistor coupled between said first voltage terminal and said matchline, said transistor being activated upon receipt of a precharge signal, thereby coupling said first voltage terminal with said matchline.

46. The processor system of claim 45, wherein said first voltage terminal comprises a VDD terminal.

47. The processor system of claim 45, wherein said first voltage terminal is coupled to a negative reference voltage terminal at a voltage level lower than VDD.

48. The processor system of claim 46, wherein said second voltage terminal is coupled to a regulated voltage source.

49. The processor system of claim 46, wherein said second voltage terminal is coupled to VDD.

50. The processor system of claim 46, wherein said CAM comprises a storage element for storing said stored bit.

51. The processor system of claim 50, wherein said storage element comprises a flip-flop for storing a true logic state of said stored bit and a complementary logic state of said stored bit.

52. A processor system, comprising:

a central processing unit;

a memory component coupled to said processor, said memory component containing a match detection circuit for a content addressable memory (CAM), said match detection circuit comprising:

a matchline switchably coupled between a first voltage terminal and a second voltage terminal, said first voltage terminal serving to precharge said matchline to a first voltage;

said matchline being configured to be connected to a second voltage level of said second terminal when a logic state of a bit stored by said CAM does not match a logic state of a bit received by said CAM for comparison with said stored bit, wherein said second voltage is greater than a ground potential and wherein said second voltage is lower than said first voltage.

53. A router, comprising:

a plurality of message receiving inputs;

a plurality of message transmitting outputs; and

a semiconductor chip containing a plurality of match detection circuits for a content addressable memory (CAM), said CAM being used to route messages on said inputs to said outputs, each of said match detection circuits comprising:

a plurality of stored bits to be compared with a corresponding plurality of input bits received by said CAM;

a matchline switchably coupled between a first voltage terminal and a second voltage terminal, said first voltage terminal serving to precharge said matchline to a first voltage level prior to said stored bits and said input bits being compared;

said matchline being coupled to said second voltage terminal when a logic state of at least one of said plurality of input bits does not match a logic state of a stored bit corresponding to said at least one input bit, said second voltage level being lower than said first voltage level and higher than a ground potential.

54. The router of claim 53, wherein each match detection circuit further comprises:

an output for outputting a first logic state when said plurality of stored bits matches said corresponding plurality of input bits received by said CAM, and for outputting a second logic state when said plurality of stored bits does not match said corresponding plurality of input bits received by said CAM.